Video apparatus

The invention relates to a video apparatus.

Patent application EP 1 128 673 describes (for instance in figure 2c) a video apparatus with a digital encoder generating a digital stream out of analogue video signals and a digital decoder generating analogue video signals based on a digital stream. In this video apparatus, a switch allows connection of the output of the digital encoder to the input of the digital decoder so that incoming analogue video signals successively go through the digital encoder and the digital decoder. This solution provides digital processing of incoming analogue video signals thanks to existing circuits of the video apparatus, and thus without extra cost.

The inventors of the present invention have found that this construction may suffer from some drawbacks in certain circumstances and propose the present invention to get rid of these drawbacks.

Notably, the present invention address a problem which could arise with this solution, as some digital encoders do not take into account some pieces of information included in the incoming analogue video signal, for instance the teletext data in the vertical blanking interval (VBI). Such pieces of information are therefore lost when going through the digital encoder and digital decoder.

The invention notably proposes a video apparatus comprising a digital encoder receiving a first analogue signal with ancillary information in a given time window and generating on an output a digital stream based at least partly on the first analogue signal, a digital decoder at least connectable to the output and generating a second analogue signal, selecting means for outputting the first analogue signal or the second analogue signal based on a control signal, and control means for determining the occurrence of said time window and correspondingly generating the control signal.

According to preferred embodiments :

- the digital decoder includes means for synchronising the second analogue signal to the first analogue signal ;
- the means for synchronising the second analogue signal to the first analogue signal are coupled to a synchronisation separator receiving the first analogue signal on an input ;
- the control means uses a first signal which is high only during periodical predetermined time intervals corresponding to said time window ;

- the first analogue signal is a CVBS signal and said first signal is high during predetermined lines of the first analogue signal ;
- the control signal is generated by a combination of the first signal and of a second periodical signal corresponding to active parts of the first analogue signal ;
- the first analogue signal is a CVBS signal, said first signal is high during predetermined lines of the first analogue signal and said second periodical signal is high during a determined part of each line ;
- the digital encoder and the digital decoder are coupled via a selector coupled to a medium interface ;
- the selecting means are coupled to an output of the video apparatus connectable to a display.

The invention also seeks to reduce cross-talk between the incoming and outgoing analogue signals. To this end, the invention also proposes a video apparatus comprising a digital encoder receiving a first analogue signal and generating on an output a digital stream based on the first analogue signal, and a digital decoder receiving the digital stream and generating a second analogue video signal based on the digital stream and synchronised with the first analogue signal.

The invention and other features thereof will be understood in the light of the following description made with reference to the attached drawing where :

- figure 1 represents a video apparatus according to the invention ;
- figures 2a and 2b are timing diagrams showing signals used in the invention ;
- figure 3 represents a second possible embodiment of the invention.

In the following description, signals are represented and described as carried on a single wire even if a plurality of wires are needed for the sake of conciseness.

Figure 1 represents a video recorder which has the ability to receive analogue video signals and to record them in a digital format, such as MPEG.

A main input 2 carries a first analogue video signal A1, for instance a CVBS signal. (Alternatively, it could be the luminance part Y of a S-Video signal.) The first analogue video signal can be incoming for instance from a tuner and demodulator, or as another example from another video apparatus through a Scart connector.

The first analogue video signal A1 contains ancillary information (for instance some text, a TV-guide, *etc.*) coded according to a given norm in predetermined periodical time windows. As an exemplary embodiment, VBI data is contained in lines 6 to 22 in odd fields and in lines 319 to 335 in even fields.

The main input is connected to a video decoder 4, for instance Philips SAA7118 that does not process or slice the VBI data but provides raw CVBS samples when VBI data is encountered.. The video decoder converts the first analogue video signal 1 into a first digital stream YC_rC_b, for instance a 4:2:2 digital stream according to the ITU-R BT.656 standard. The first digital stream YC_rC_b output from the video decoder 4 is input to a MPEG encoder 6 where it is converted into a MPEG digital stream. The MPEG encoder 6 does not process the raw digitised teletext data from video decoder 4.

The MPEG digital stream therefore represents the same video sequence as the first analogue video signal A1, but in a digital format. The output of the MPEG encoder 6 carrying the MPEG digital stream is connected to a selector 7 which is in turn connected on the one hand to a hard disk drive 10 and to a MPEG decoder 8. The hard disk drive 10 is a possible medium interface, but of course other types of medium interface such as DVD-recorder or D-VHS recorder could be used instead.

As explained in EP 1 128 673, the selector 7 allows to connect the MPEG encoder 6 to the hard disk drive 10 and to the MPEG decoder 8 and to connect the hard disk drive 10 to the MPEG decoder 8. The medium interface 10 can thus record on the medium the MPEG stream generated by the MPEG encoder 6, or read the medium and output a MPEG stream to the MPEG decoder 8 in order to play-back a video sequence.

Furthermore, thanks to the selector 7, the MPEG digital stream out of the MPEG encoder 6 can thus be transmitted to the digital decoder 8, for instance a Sti5519 incorporating a MPEG decoder and a video encoder.

In this case, the digital decoder 8 (and particularly its video encoder part) outputs a second analogue video signal A2 (for instance according to the CVBS standard) which represents the same video sequence as the first analogue video signal A1, but with some changes and delay (about 600 ms) due to digital signal processing through circuits 4, 6 and 8.

The digital decoder 8 receives field identification information FID from the video decoder 4. The digital decoder 8 also receives horizontal reference pulses H and vertical reference pulses V from a synchronisation

separator 12 which extracts these pulses from the first analogue video signal A1 on main input 2.

By using these horizontal and vertical reference pulses H,V, the video encoder part of the digital decoder 8 generates the second analogue video signal A2 synchronised with the first analogue video signal A1. As the second analogue video signal A2 is delayed compared to the first analogue video signal A1 as already mentioned, this means that, at any time, the first and second analogue video signals A1, A2 define lines having same number but belonging to two different pictures.

Video decoder 4 provides a field identification signal FID to indicate which field is currently received and digitised (odd or even field). In this particular instance, a low level indicates an odd field (Field1) and a high level indicates an even field (Field2).

The main input 2 carrying the first analogue video signal A1 is connected to a first input of a switch 20 through a clamping circuit 16. Similarly, the video output of the digital decoder 8 carrying the second analogue video signal A2 is connected to a second input of the switch 20 through a clamping circuit 18. The clamping circuits 16 and 18 allow to have a common black level on the two inputs of the switch 20.

The digital decoder 8 also generates a VBI-occurrence signal VBI and a fast-blanking signal FBL which are transmitted to an AND-gate 14 which in turn generates a control signal CTL controlling the switch 20.

The VBI-occurrence signal VBI is indicative of time windows when the ancillary information should be present in the second analogue video signal A2 according to the norm (line 6 to 22 or line 319 to 335 depending on the field), which correspond to time windows where ancillary information is present in the first analogue video signal A1 as the two signals A1 and A2 are synchronised (see above).

The fast-blanking signal FBL is a line-frequent signal which allows to consider only the active part of the lines, as further explained below.

The control signal CTL resulting from the logical AND combination of the VBI-occurrence signal VBI and the fast-blanking signal FBL is thus indicative of (*i.e.* high) when VBI data is present in the first analogue video signal A1.

Switch 20 outputs on a main output 22 the clamped second analogue video signal A2 when the control signal CTL is low and the clamped first analogue video signal A1 when the control signal CTL is high. The main

output 22 is for instance implemented by pins of a Scart connector to be connected to a display.

The main output 22 thus carries as analogue video signal the digitally-processed video signal with re-inserted VBI data, even if the digital encoder (video decoder) cannot deal with such VBI data.

As previously explained, the VBI data in the video signal on main output 22 is not inserted in the same picture as originally (*i.e.* in the first analogue video signal A1), but this causes no problem, as VBI data are not accurately related to the picture where they are inserted and as the delay is anyway less than 1 s.

Hence, thanks to this construction, it can be taken advantage both of digital signal processing and of ancillary information with any kind of digital encoder.

Furthermore, as the second analogue video signal A2 (output of digital decoder 8) is synchronised to the first analogue video signal A1 (input of digital encoder 4), cross-talk between these two signals is greatly reduced to the benefit of the quality of the generated pictures.

Figures 2a and 2b represent timing diagrams of the VBI-occurrence signal VBI, of the fast-blanking signal FBL and of the first analogue video signal A1 respectively in an odd field (Field1) and in an even field (Field2).

The VBI-occurrence signal VBI is active (high) for the 17 lines during which the VBI information is present (lines 6 to 22 for odd fields and lines 319 to 335 for even fields), *i.e.* for a period of 1 088 µs in each field. The fast-blanking signal FBL is high for each line only where data information is present, *i.e.* during 52 µs out of 64 µs.

By combining the VBI-occurrence signal VBI and the fast-blanking signal FBL in an AND-gate as explained above, the resulting control signal CTL is thus accurately indicative of when VBI data should be present in the second analogue video signal A2 and is present in the first analogue video signal A1, as these two signals are synchronised with each other.

The use of the fast-blanking signal FBL allows to accurately insert in the second analogue video signal A2 only the data information contained in the first analogue video signal A1, and not other parts of the signal, such as colour burst.

In an alternative embodiment of the invention, the VBI-occurrence signal VBI as such could be used as a control signal for switch 20. The insertion of VBI data from the first analogue video signal A1 into the second

analogue video signal A2 would then also take place, but this must be done carefully to ensure that the VBI portion from A1 is matched properly to the other video portion of A2 in terms of the black level, H-sync pulse and colour burst. Otherwise, some problems such as line synchronisation may arise when the output video signal is supplied to a TV.

In figure 1, the field identification information FID, the horizontal reference pulse H and the vertical reference pulse V are represented as directly input to the digital decoder 8. However, it should be noted that a further circuit for re-shaping these signals could be inserted without departing from the scope of the invention.

An alternative embodiment of the invention is illustrated at figure 3. References used in figure 1 are kept the same for circuit or signals which are the same or have the same function as in the embodiment of figure 1. The main difference in the present embodiment compared to the embodiment of figure 1 is that a control circuit 26 is used to generate and send a control signal CTL to the switch 20 based on a combined field identification and horizontal synchronisation signal FID/H received from the video decoder 4.

The control circuit 26 is for instance a FPGA (Field Programmable Gate Array). The generated control signal CTL has a shape corresponding to the shape of the signal CTL in the embodiment of figure 1.

The FPGA 20 is also used for re-shaping and time-base correction of the combined signals FID/H and therefore outputs corrected combined signals FID/H' to the digital decoder 8 for synchronisation with the incoming analogue signal A1.

With this construction, as in the first embodiment, the second analogue video signal A2 (generated by the digital decoder 8) is synchronised with the first analogue video signal A1. This means that, even if the video sequence represented by the second analogue video signal A2 is shortly delayed compared to the video sequence represented by the first analogue video signal A1, both signals A1 and A2 represent the same line for display at a given moment in time (but for different fields).

Furthermore, as in the first embodiment, the switch 20 controlled by the control signal CTL allows to insert information from the VBI of the first analogue video signal A1 into the second analogue video signal A2.

It can also be noted that the second embodiment includes a further source of digital stream, here a IEEE 1394 interface 24. The user can select this source of data (via a user interface and a microprocessor of the apparatus)

by switching a digital switch 25 to connect the IEEE 1394 interface to the MPEG encoder 6. In this case, the teletext information contained in the VBI of the incoming analogue signal A1 can be inserted in the analogue signal built from the IEEE 1394 digital stream and used by the display to be connected to output 22.